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REMARKS

This Amendment is in response to the Office Action mailed on September 5, 2006. Claims 1-7 are cancelled without prejudice or disclaimer. Claims 8-17 are new. The title and the abstract of the specification are amended editorially. No new matter is added. Claims 1-4 and 8-17 are pending.

New Claims:

Claims 8-17 are new. Claim 8 is added and includes the features of claim 1 and is further supported, for example, in the specification at page 12, lines 2-27 and Figures 2 and 3. Claim 9 is added and includes the features of claim 2 and is further supported, for example, in the specification at page 12, lines 2-27 and Figures 2 and 3. Claim 10 is added and includes the features of claim 3 and is further supported, for example, in the specification at page 12, lines 2-27 and Figures 2 and 3.

Claim 11 is added and includes the features of claim 1 and is further supported, for example, in the specification at page 17, line 21-page 18, line 24 and Figures 16 and 17. Claim 12 is added and includes the features of claim 2 and is further supported, for example, in the specification at page 17, line 21-page 18, line 24 and Figures 16 and 17. Claim 13 is added and includes the features of claim 3 and is further supported, for example, in the specification at 17, line 21-page 18, line 24 and Figures 16 and 17.

Claims 14-16 are added and include the features of claims 1 and 4 and are further supported, for example, in the specification at page 19, line 10-page 21, line 10 and Figures 19-25.

Claim 17 is added and includes the features of claims 1 and 4 and is further supported, for example, in the specification at page 13, line 25-page 16, line 7 and Figures 7-11.

Objections to the Specification:

The abstract is objected to for improper format. The abstract is amended to be limited to a single paragraph on a separate sheet within the range of 50 to 150 words. Withdrawal of the objection is requested.

§112 Rejections:

Claims 3 and 4 are rejected as being indefinite and as lacking enablement. Claims 3 and 4 are cancelled without prejudice or disclaimer, rendering this rejection moot. New claims 8-17 point out and distinctly claim the subject matter of this invention and also are commensurate in scope with the specification to provide enablement to those skilled in the art to make and use this invention. Withdrawal of these rejections is requested.

§102(b) Rejections:

Claims 1-3 are rejected as being anticipated by Atsunori (JP Publication No. 2002-050501). Claims 1-3 are cancelled without prejudice or disclaimer, rendering this rejection moot. Withdrawal of this rejection is requested.

§103(a) Rejections:

Claim 4 is rejected as being obvious over Atsunori (JP Publication No. 2002-050501). Claim 4 is cancelled without prejudice or disclaimer, rendering this rejection moot. Withdrawal of this rejection is requested.

New Claims:

Claims 8-17 are newly added. However, to expedite the prosecution of this case the following distinctions over Atsunori are noted. Claim 8 is directed to a chip resistor that requires, among other features, a pair of lower end recesses each formed directly on a lower surface of a resistor metal plate adjacent to a respective one of the end surfaces of the resistor metal plate and a pair of connection terminal electrodes each formed in a respective one of the lower end recesses. Claim 8 also requires an upper insulating layer formed on the upper surface of a resistor metal plate without covering the end surfaces of the resistor metal plate and a lower insulating layer formed on the lower surface of the resistor metal plate between the connection terminal electrodes without covering the end surfaces of the resistor metal plate.

Nowhere does Atsunori teach or suggest these features. First, nowhere does Atsunori teach or suggest two insulating layers, an upper insulating layer and a lower insulating layer, neither of which covers the end surfaces of the resistor metal plate. In

contrast, Atsunori is directed to a mounting object for mounting a chip resistor for current detection in a substrate that includes a resistor section (5) enclosed in only a single insulating layer (6) (see paragraphs [0012] and [0040] and Figures 1, 3, 6 and 7). Moreover, the insulating layer (6) completely covers the end surfaces of the resistor section (5) (see Figure 3). Second, nowhere does Atsunori teach or suggest a pair of lower end recesses each formed directly on a lower surface of a resistor metal plate adjacent to a respective one of the end surfaces of the resistor metal plate with a connection terminal electrode formed in each recess. Atsunori merely includes an insulating layer (6) that has a lower surface which is formed with a pair of end recesses, in which the terminal sections (4) are bent inwardly to be received. However, nowhere does Atsunori include a resistor section (5) that is formed with a single recess (see Figure 1).

Claim 11 is directed to a chip resistor that requires, among other features, a lower intermediate recess formed directly on the lower surface of the resistor metal plate between the end surfaces of the resistor metal plate. Claim 11 also requires an upper insulating layer formed on the upper surface of a resistor metal plate without covering the end surfaces of the resistor metal plate and a lower insulating layer formed in the lower intermediate recess between the connection terminal electrodes without covering the end surfaces of the resistor metal plate.

Nowhere does Atsunori teach or suggest these features. First, nowhere does Atsunori teach or suggest two insulating layers, an upper insulating layer and a lower insulating layer, both of which do not cover the end surfaces of the resistor metal plate. As discussed above, Atsunori is directed to a mounting object for mounting a chip resistor for current detection in a substrate that includes a resistor section (5) enclosed in only a single insulating layer (6) (see paragraphs [0012] and [0040] and Figures 1, 6 and 7). Moreover, the insulating layer (6) completely covers the end surfaces of the resistor section (5) (see Figure 3). Second, nowhere does Atsunori teach or suggest a lower intermediate recess formed directly on the lower surface of the resistor metal plate between the end surfaces of the resistor metal plate. Atsunori merely includes an insulating layer (6) that has a lower surface which is formed with a pair of end recesses,

in which the terminal sections (4) bent inwardly are received. However, nowhere does Atsunori include a resistor section (5) that is formed with a single recess (see Figure 1).

Claim 14 is directed to a method of making chip resistors that requires, among other features, the step of covering the upper and lower surfaces of the metal plate blank with upper and lower insulating layers, such that the chip resistor has an upper insulating layer formed on the upper surface of a resistor metal plate without covering the end surfaces of the resistor metal plate and a lower insulating layer formed in a lower intermediate recess of the resistor metal plate without covering the end surfaces of the resistor metal plate.

Nowhere does Atsunori teach or suggest these features. In particular, nowhere does Atsunori teach or suggest the step of covering the upper and lower surfaces of the metal plate blank with upper and lower insulating layers, such that the chip resistor has an upper insulating layer formed on the upper surface of a resistor metal plate without covering the end surfaces of the resistor metal plate and a lower insulating layer formed in the lower intermediate recess between the connection terminal electrodes without covering the end surfaces of the resistor metal plate. As discussed above with regards to claim 11, Atsunori is directed to a mounting object for mounting a chip resistor for current detection in a substrate that includes a resistor section (5) enclosed in only a single insulating layer (6) (see paragraphs [0012] and [0040] and Figures 1, 6 and 7). Moreover, the insulating layer (6) completely covers the end surfaces of the resistor section (5) (see Figure 3). Therefore, the step of covering the upper and lower surfaces of the metal plate blank with upper and lower insulating layers without covering the end faces cannot be taught or suggested by Atsunori.

Claim 17 is directed to a method of making chip resistors that requires, among other features, the step of cutting grooves in the lower surface of the metal plate blank and the step of covering an upper surface of the metal plate blank with an upper insulating layer while forming a lower insulating layer in each of the grooves. This allows a chip resistor to be made that includes an upper insulating layer formed on the upper surface of a resistor metal plate without covering the end surfaces of the resistor metal plate and a lower insulating layer formed on the lower surface of the resistor metal plate between connection terminal electrodes without covering the end surfaces of the

resistor metal plate.

Nowhere does Atsunori teach or suggest these features. In particular, nowhere does Atsunori teach or suggest the step of cutting grooves in the lower surface of the metal plate blank and the step of covering an upper surface of the metal plate blank with an upper insulating layer while forming a lower insulating layer in each of the grooves. As discussed above, Atsunori discloses a mounting object for mounting a chip resistor for current detection in a substrate that discloses a resistor section (5) enclosed in only a single insulating layer (6) (see paragraphs [0012] and [0040] and Figures 1, 3, 6 and 7). Moreover, the insulating layer (6) completely covers the end surfaces of the resistor section (5) (see Figure 3). Therefore, the step of covering the upper and lower surfaces of the metal plate blank with upper and lower insulating layers without covering the end faces cannot be taught or suggested by Atsunori.

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Conclusion:

Applicants respectfully assert that claims 8-17 are now in condition for allowance. If a telephone conference would be helpful in resolving any issues concerning this communication, please contact Applicants' primary attorney-of record, Douglas P. Mueller (Reg. No. 30,300), at (612) 455-3804.

Respectfully submitted,

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